50-GHZ INTERCONNECT DESIGN IN STANDARD SILICON TECHNOLOGY

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ABSTRACT

Coplanar waveguides were fabricated in a process that emulates silicon CMOS technologies with 5 to 10 metal layers. The observed S_{21} loss of 0.3dB/mm at 50 GHz is among the lowest ever reported with standard Al interconnects on Si/SiO_2. Optimum design parameters were counter-intuitive: in some frequency ranges, the lowest loss was achieved with relatively *narrow* lines over a *low-resistivity* substrate. This was exploited in the design of transmission lines that are fully compatible with a CMOS technology. The process emulation was calibrated with a commercial 4-layer Al/Cu CMOS technology.

INTRODUCTION

Recently, there has been a great deal of interest to extend digital CMOS into GHz operations and to use standard CMOS for monolithic RF circuits[1]. However, the viability of high-speed interconnects in Si technology has been questioned due to the losses in the Si substrate, the SiO_2 layer and the metal lines. Various solutions involving a high-resistivity substrate have therefore been proposed[2]-[6], but they are not compatible with standard CMOS technology where a low-resistivity substrate with a thin epi-layer is preferred to reduce latchup and enhance yield[7]. Nevertheless, due to the rapid increase in the number of interconnects, the top level metals will be situated further away from the Si substrate as the technology scales, thus reducing the losses (Fig. 1).

EXPERIMENT

An experiment was conducted to emulate state-of-the-art and future Si CMOS technologies. Low- and high-resistivity (0.5 and 15Ω-cm) Si substrates were used, and LPCVD SiO_2 (4, 8, 12 and 16μm) was deposited. Coplanar waveguides (CPW) were fabricated with 2-μm thick Al metallization (Fig. 2).

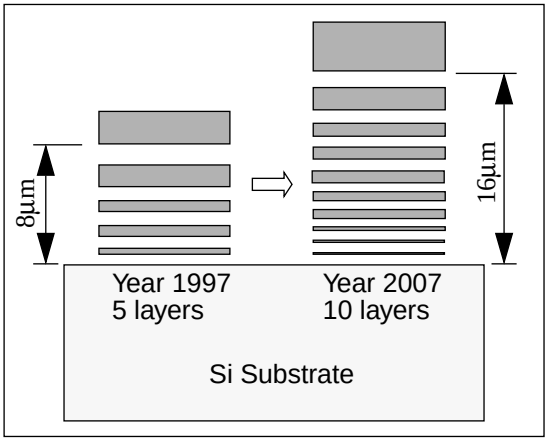

Fig. 1. Approximate trend of interconnect stack.

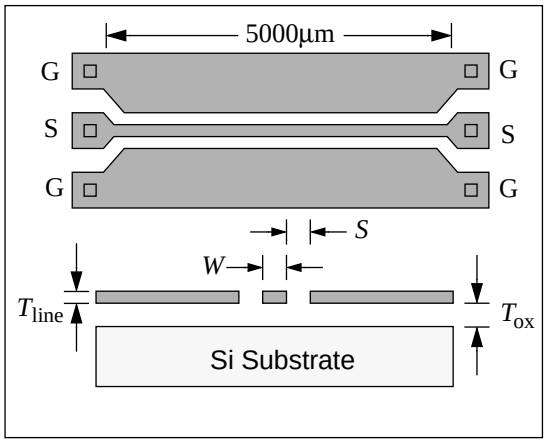

Fig. 2. Top and cross-sectional views of a CPW line.

Although future interconnection schemes are likely to incorporate Cu and low-ε_r dielectrics, Al and SiO_2 were adopted in our study. This technology is readily available and yields conservative results. The layout dimensions of the CPW lines were derived from calculations and 2D simulations[8],[9]. The substrate resistivity and T_{ox} dependences were ignored in the calculations for a high-resistivity substrate shown in

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Table 1. More accurate modeling[9] confirmed that the impedance of the lines with small coupling to the substrate was adequately predicted by the simple calculations. A wide range of impedances, Z_0, were implemented.

TABLE 1. CPW Spacing, *S*, for various *W* and Z_0.

	IMPEDANCE (Z_0)		
WIDTH	**40 Ω**	**60 Ω**	**90 Ω**
5μm	1.25μm	5μm	20μm
10μm	2.5μm	10μm	40μm
20μm	5μm	20μm	80μm
40μm	10μm	40μm	160μm

The *S*-parameters were measured with an HP8510C Network Analyzer and Cascade coplanar ground-signal-ground (G-S-G) probes. Reference open pads were used to subtract the pad parasitics, and relatively long lines (5mm) were used in order to obtain accurate measurements.

RESULTS AND DISCUSSION

The *S*-parameters for a range of line widths with the same impedance (40Ω) revealed some interesting results (Fig. 3). The 40μm wide line has the lowest loss below 10 GHz but the *highest* loss above 30 GHz. The *S*-parameters for the 10μm wide line are shown for two different impedances (40Ω and 90Ω)

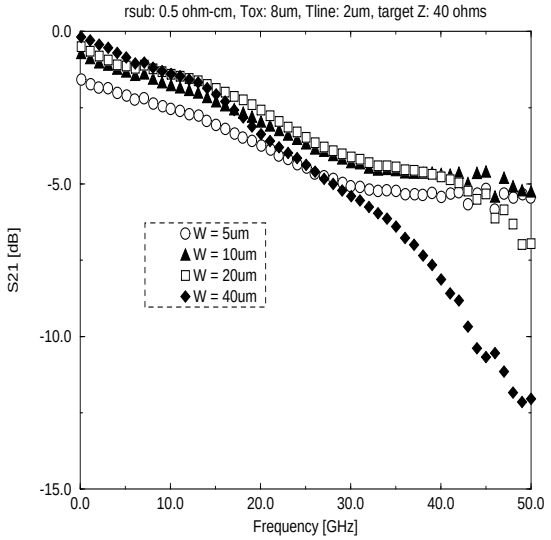

Fig. 3. S_{21} for CPW with various widths.

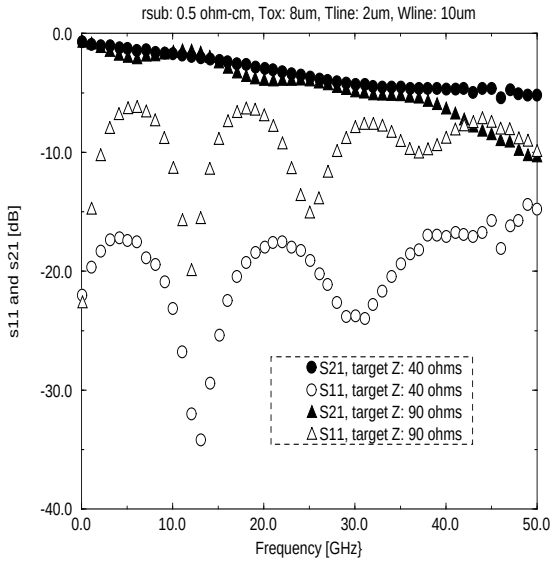

Fig. 4. *S*-parameters for CPWs with different target Z_0.

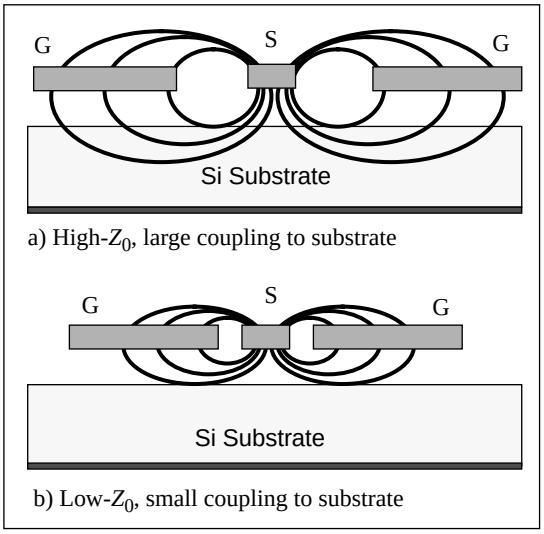

Fig. 5. CPW cross-sections illustrating electric field lines.

in Fig 4. The loss characteristics are similar to those of the wide lines in Fig. 3: the loss increases significantly above 30 GHz due to the large coupling through the substrate. This coupling is illustrated with a sketch of the electric field lines in Fig.5. The coupling through the substrate is more significant when the width or space of the line is larger than T_{ox}. Note that at high frequencies, the backside substrate contact is not effective due to the large inductance of the return path: the electric field lines that penetrate into the substrate will terminate on the low-inductance coplanar grounds.

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A circuit model was developed to aid the understanding. Assuming small SiO_2 dielectric losses, the RC components of the CPW line admittance were selected to represent the actual layout (Fig. 6). The frequency-dependent parameters were extracted from the data, and the series combination of ($C_{sub} \parallel R_{sub}$) and C_{eff} was fitted to match the admittance[10]-[13] (Fig. 7). A reasonable fit with the experimental data was achieved (Fig. 8). Note that the real part of the propagation constant, Re(γ), was *smaller* (i.e., lower loss) for the *low-resistivity* substrate below 20 GHz. This was intriguing since previous work has only strived to obtain lower loss

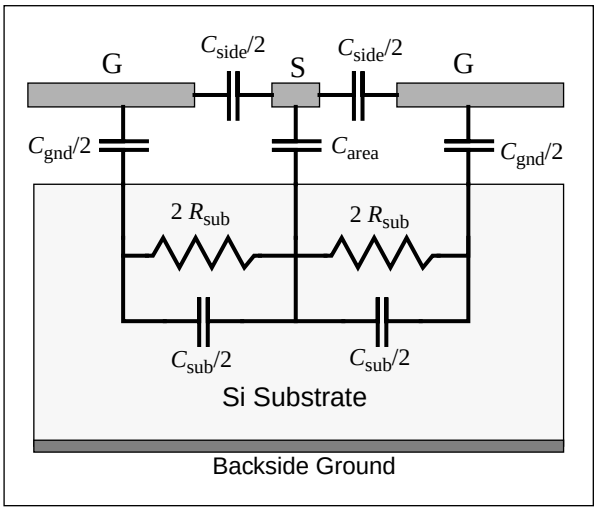

Fig. 6. Illustration of RC components of CPW line.

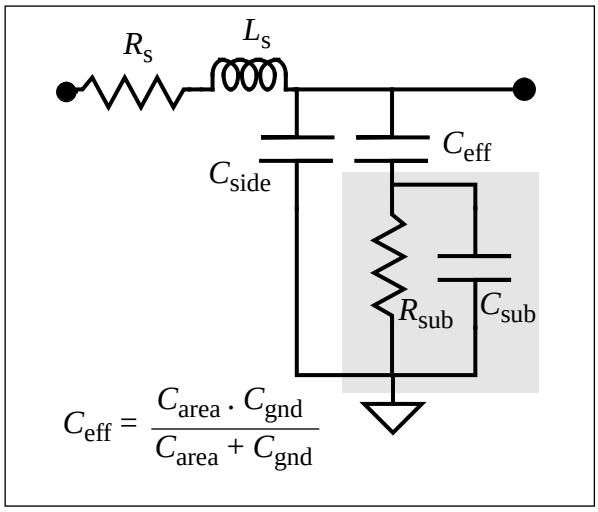

Fig. 7. Elements of distributed RLC model of CPW.

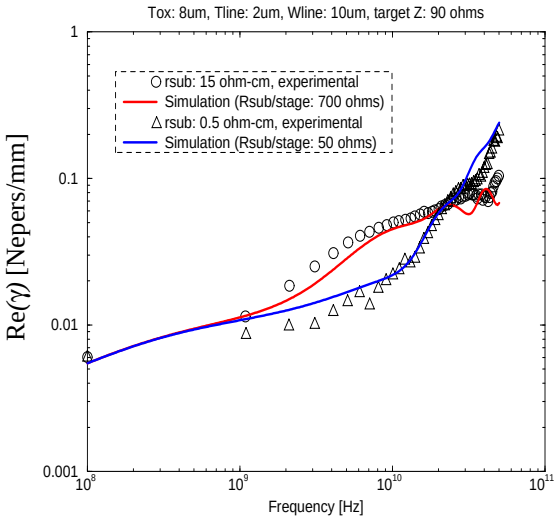

Fig. 8. Propagation constant, γ, for CPW lines.

by using *high-resistivity* substrates [3]-[6],[11]-[12]. Furthermore, simulations with the extracted model indicated that the loss could be reduced even further by reducing R_{sub}. CMOS epi-wafers typically have a bulk resistivity of 20mΩ-cm which is 25x lower than our 'low-resistivity' substrates. To examine the extreme of a low-resistivity wafer, a 0.5μm thick metal ground plane was inserted beneath the SiO_2 layer. The S_{21} loss with the metal ground shield for the 5-metal layer emulation was only 0.6dB/mm at 50 GHz, and for a future 10-metal-layer technology, S_{21} was as low as 0.3dB/mm (Fig. 9). Due to the reduced coupling to the substrate/shield, a wider line could be used. This also supports the assumption of small SiO_2 dielectric losses - contrary to other observations[5].

The emulation of the advanced processes was verified with a comparison to a 4-metal-layer industry CMOS process from Hewlett-Packard (HP). Due to area constraints, a shorter coplanar stripline (CPS) was used (Fig. 10). Furthermore, the ground line was also narrower than the structures fabricated at Stanford University (SU). Since the ground return current tends to crowd near the signal line at high frequencies, the width of the ground line should not affect the comparison significantly. The distance to M4 in the HP process is about 4.4μm, and the SU wafers with T_{ox}= 4μm yield the best match (Fig.11). The higher loss (~3x) in the HP process is primarily attributed to the relatively thin metal line (1.2μm Al/Cu vs. 2μm 100% Al). The

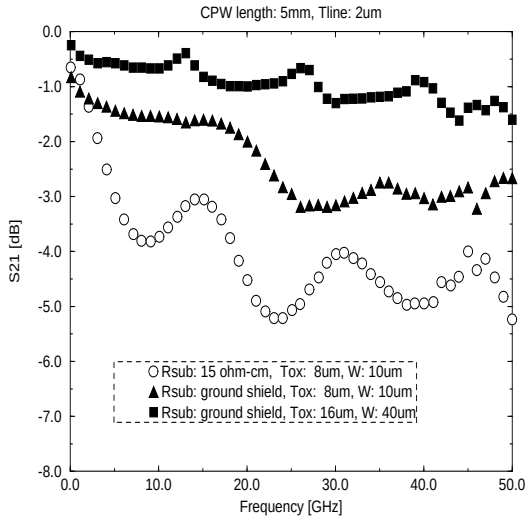

Fig. 9. S_{21} for various CPW lines.

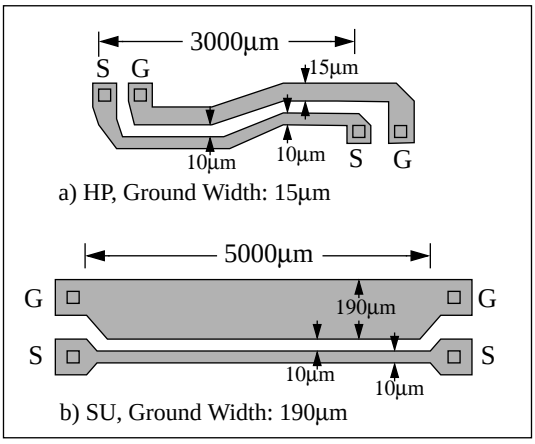

Fig. 10. Top view of the CPS lines.

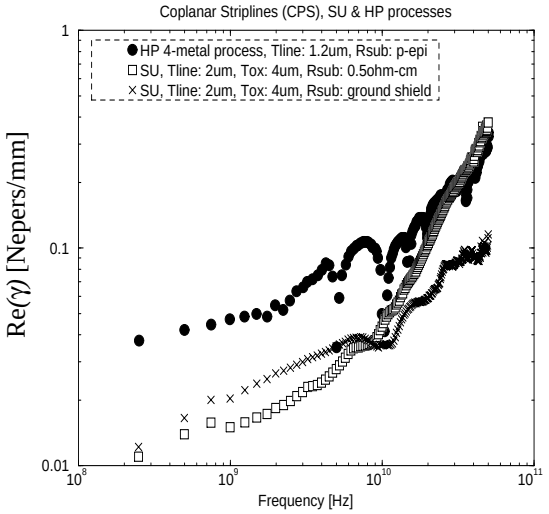

Fig. 11. Propagation constant, γ, for CPS lines.

impedances are similar: 65Ω at 1 GHz. Note that the trend of loss vs. frequency resembles more closely the SU with ground shield, whereas the loss for the SU with 0.5Ω-cm substrate has a steeper increase vs. frequency.

CONCLUSION

Two techniques of achieving low-loss coplanar waveguides were demonstrated: 1) reduce line widths and spacing to avoid substrate coupling and 2) use low-resistivity substrate or metal/poly/diffusion to provide a low resistance for the lateral ground connection. The loss is expected to be further reduced with the increasing number of interconnects and thicker, lower-resistivity top-level metallization in future technologies.

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